What Is Claimed Is:

1. A method of delaying a ready signal from an emulation system, configured for emulating a network device, to a central processing unit (CPU) for initiating an access cycle of the CPU, the emulation system being configured for operating according to an emulation clock having a maximum speed substantially less than a prescribed operating speed of the CPU, the method comprising:

providing a programmable device,

receiving, at the programmable device, a ready signal sent from the emulation system,

delaying the ready signal in the programmable device based on the emulation clock; and

sending the delayed ready signal to the CPU based on the emulation clock, the delayed ready signal enabling the emulation system to complete the access cycle of the CPU prior to the CPU initiating processing of subsequent instructions.

2. The method of claim 1, wherein the emulation system is configured for emulating a multiport switch having switch ports.

3. The method of claim 2, wherein the CPU is configured to operate at approximately 40 MHz and the emulation clock is configured to operate at approximately 250 KHz.

4. A system for delaying a ready signal from an emulation system, configured for emulating a network device, to a central processing unit (CPU) for initiating an access cycle of the CPU, the system comprising:

an emulation system,

a central processing unit (CPU), the emulation system being configured for operating according to an emulation clock having a maximum speed substantially less than a prescribed operating speed of the CPU, and

a programmable device configured for receiving a ready signal from the emulation system, delaying the ready signal based on the emulation clock, and sending the delayed ready signal to the CPU based on the emulation clock, the delayed ready signal enabling the emulation system to complete the access cycle of the CPU prior to the CPU initiating processing of subsequent instructions.

5. The system of claim 4, wherein the emulation system is configured for emulating a multiport switch having switch ports.

6. The system of claim 5, wherein the CPU is configured to operate at approximately 40 MHz and the emulation clock is configured to operate at approximately 250 KHz.